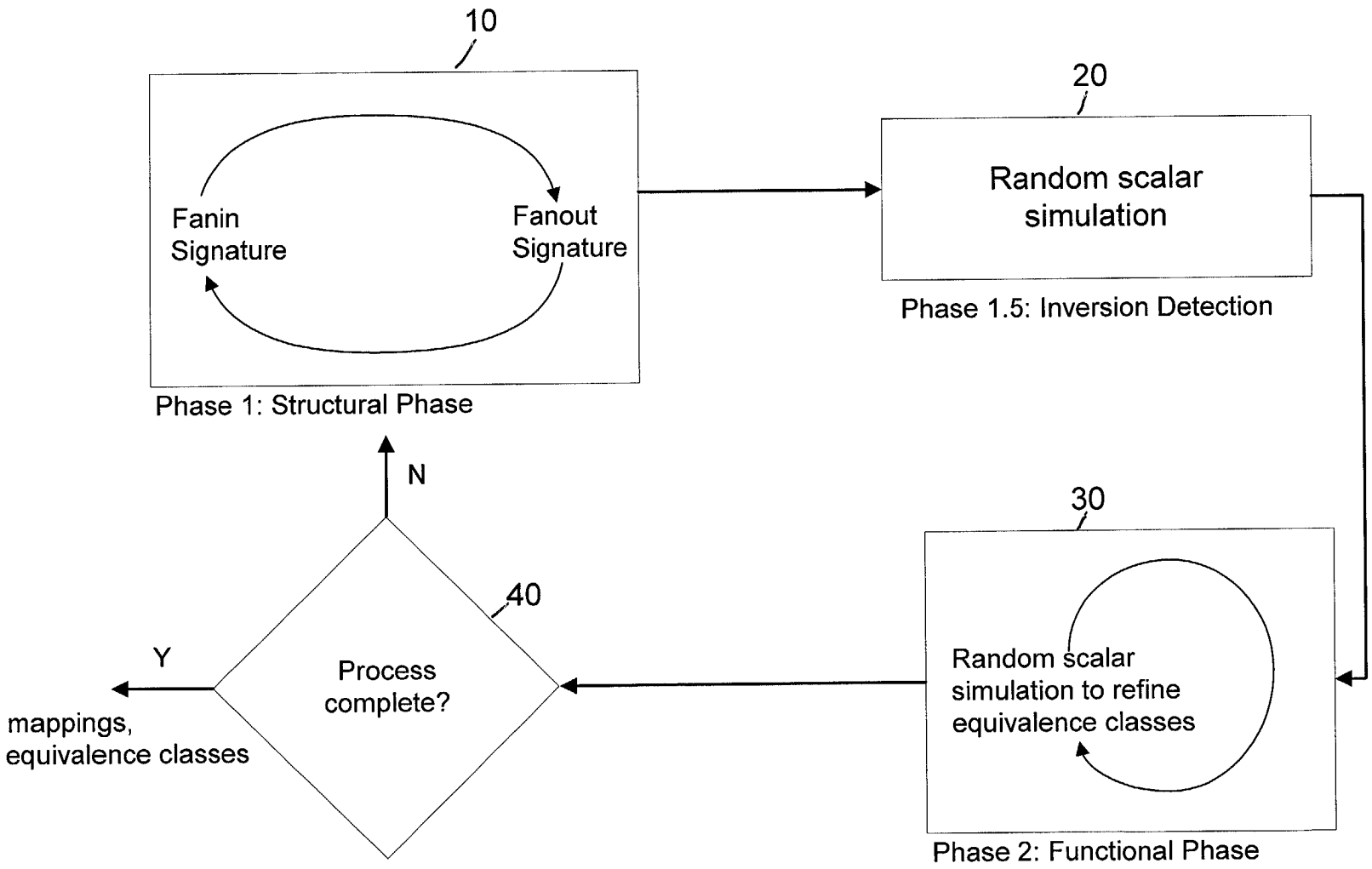
FIG. 1



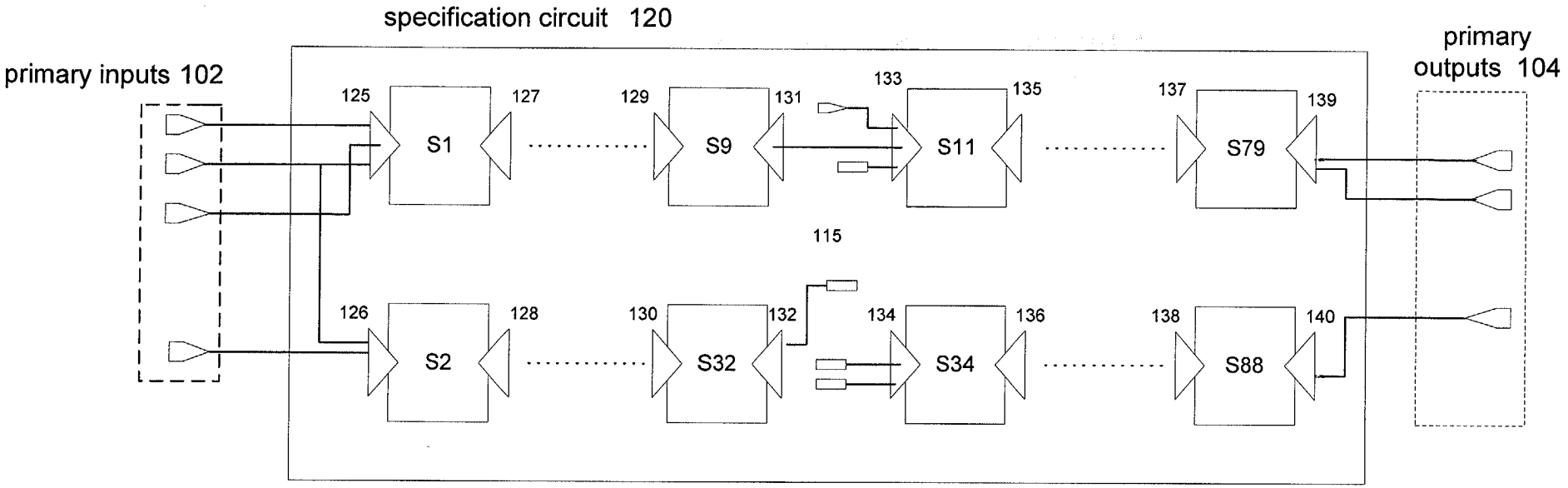
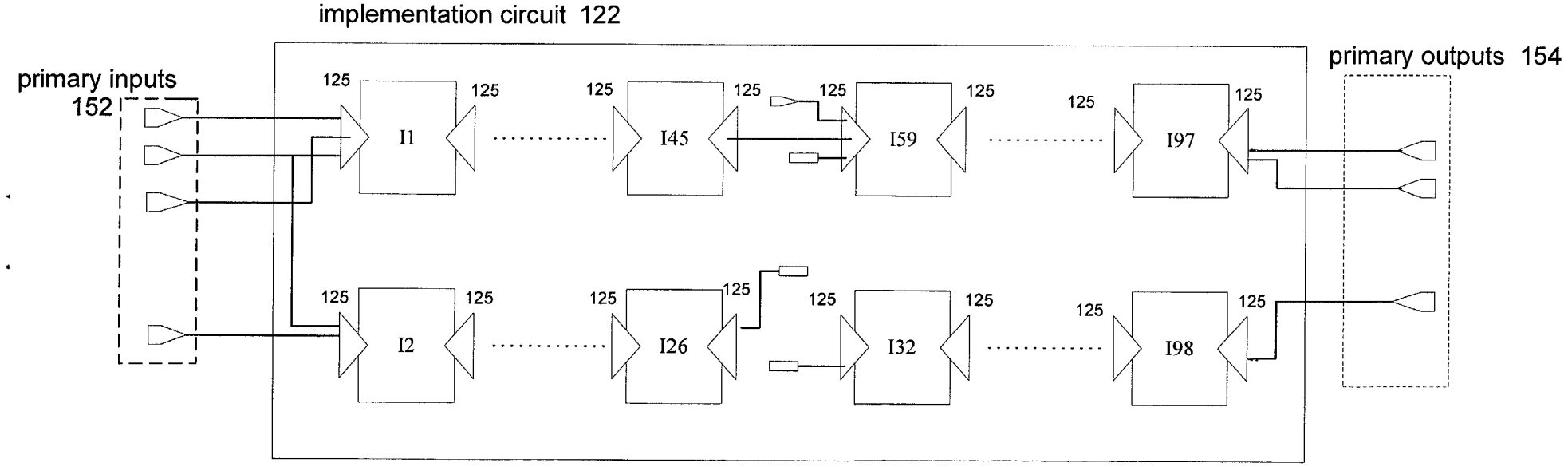
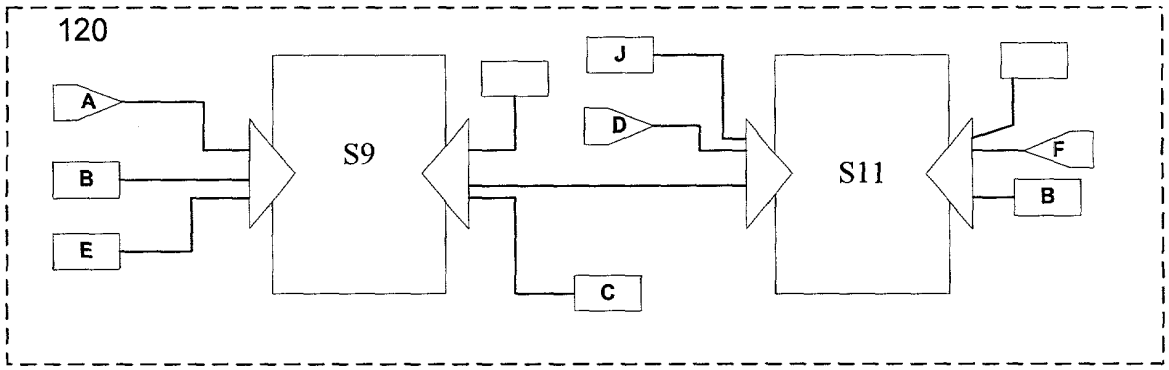

specification circuit 120
primary inputs 102
primary outputs 104
125
127
129
131
133
135
137
139
S1
S9
S11
S79
115
126
128
130
132
134
136
138
140
S2
S32
S34
S88

FIG. 2


implementation circuit 122
primary inputs
152
primary outputs 154
125
I1
I45
I59
I97
I2
I26
I32
I98



STAGE 1

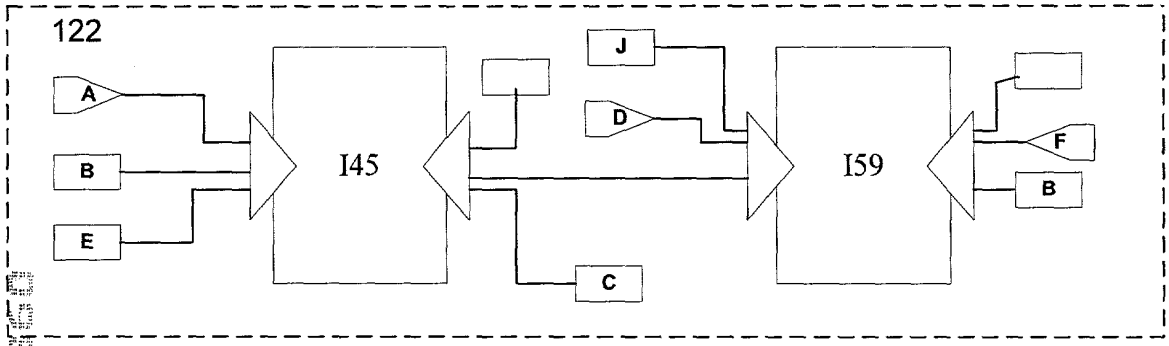
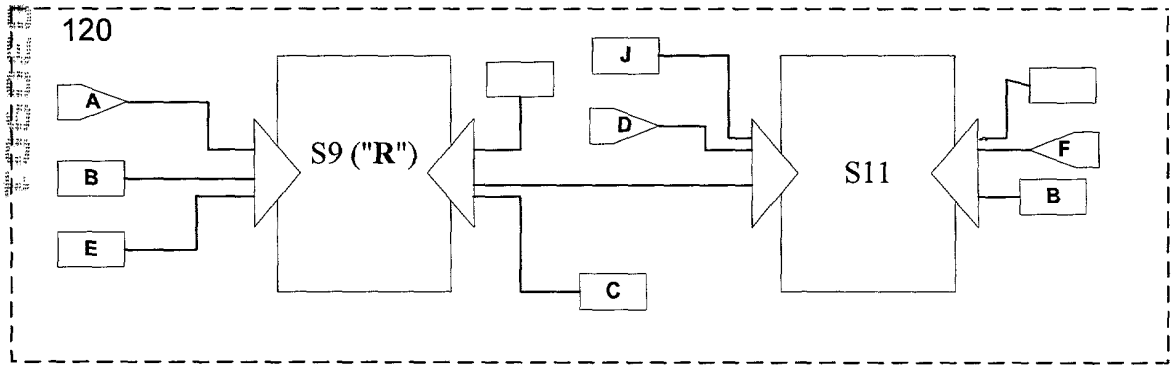


FIG. 3a



STAGE 2

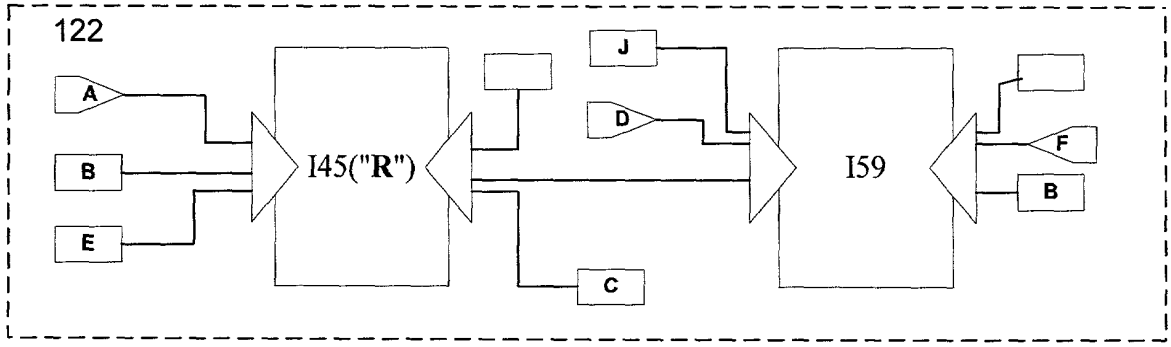


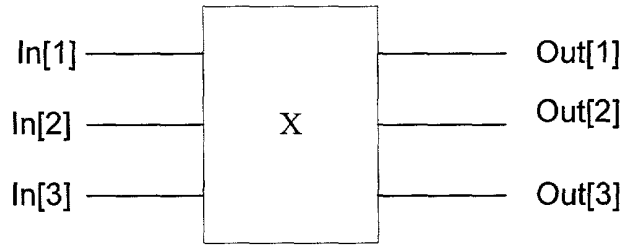
FIG. 3b

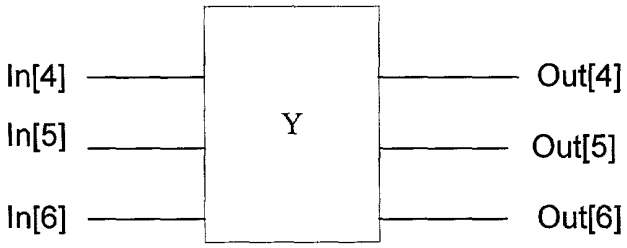
FIG. 4

Fanin signatures		Fanout signatures	
ABE	DJ	C	BF
S9	S11	S9	S11
I45	I59	I45	I59
	S7	S57	S29
	I35	I14	I8
		S80	S64
		I26	I53
		I75	
		I76	

Fanin signatures		Fanout signatures	
ABE	DJR	C	BF
S9	***S11***	S9	S11
I45	***I59***	I45	I59
		S57	S29
		I14	I8
		S80	S64
		I26	I53
		I75	
		I76	

FIG. 5





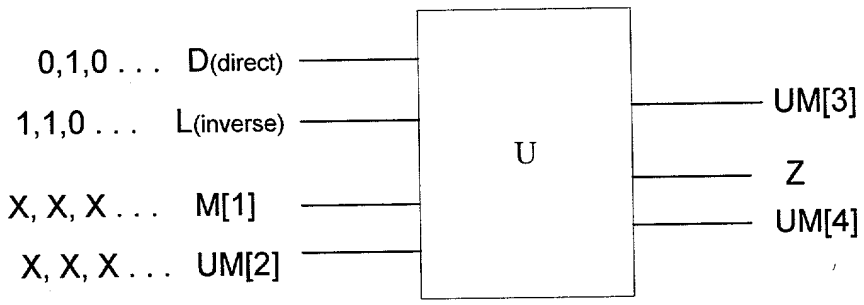
250

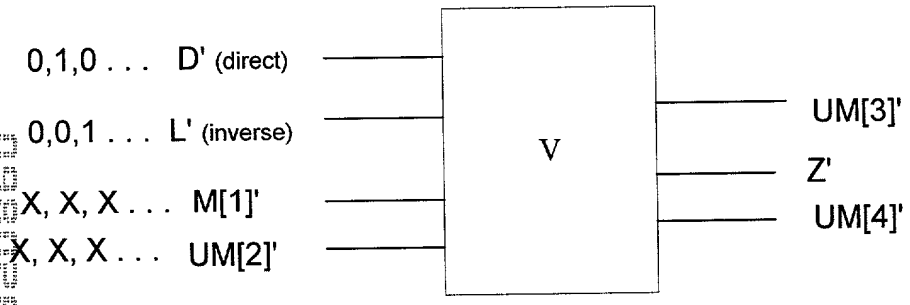
In[1]	In[2]	In[3]	Out[1]	Out[2]	Out[3]
0	0	0	0	1	0
0	0	1	1	1	1
0	1	0	0	1	1
0	**1**	**1**	**1**	**0**	**1**
1	0	0	0	0	0
1	**0**	**1**	**1**	**0**	**1**
1	1	0	1	1	0
1	1	1	0	1	0

255

In[4]	In[5]	In[6]	Out[4]	Out[5]	Out[6]
0	0	0	0	1	0
0	0	1	1	1	1
0	1	0	0	1	1
0	**1**	**1**	**0**	**1**	**1**
1	0	0	0	0	0
1	**0**	**1**	**0**	**0**	**1**
1	1	0	1	1	0
1	1	1	0	1	0

FIG. 6





270

	D	L	D'	L'	M[1]	M[1]'	UM[1]	UM[1]'	Z	Z'
1	0	1	0	0	X	X	X	X	0	1
2	1	1	1	0	X	X	X	X	1	0
3	0	0	0	1	X	X	X	X	0	1
.										
.										
.										
30	1	0	1	1	X	X	X	X	0	1
31	0	1	0	0	X	X	X	X	0	1
32	1	0	1	1	X	X	X	X	X	X

FIG. 7

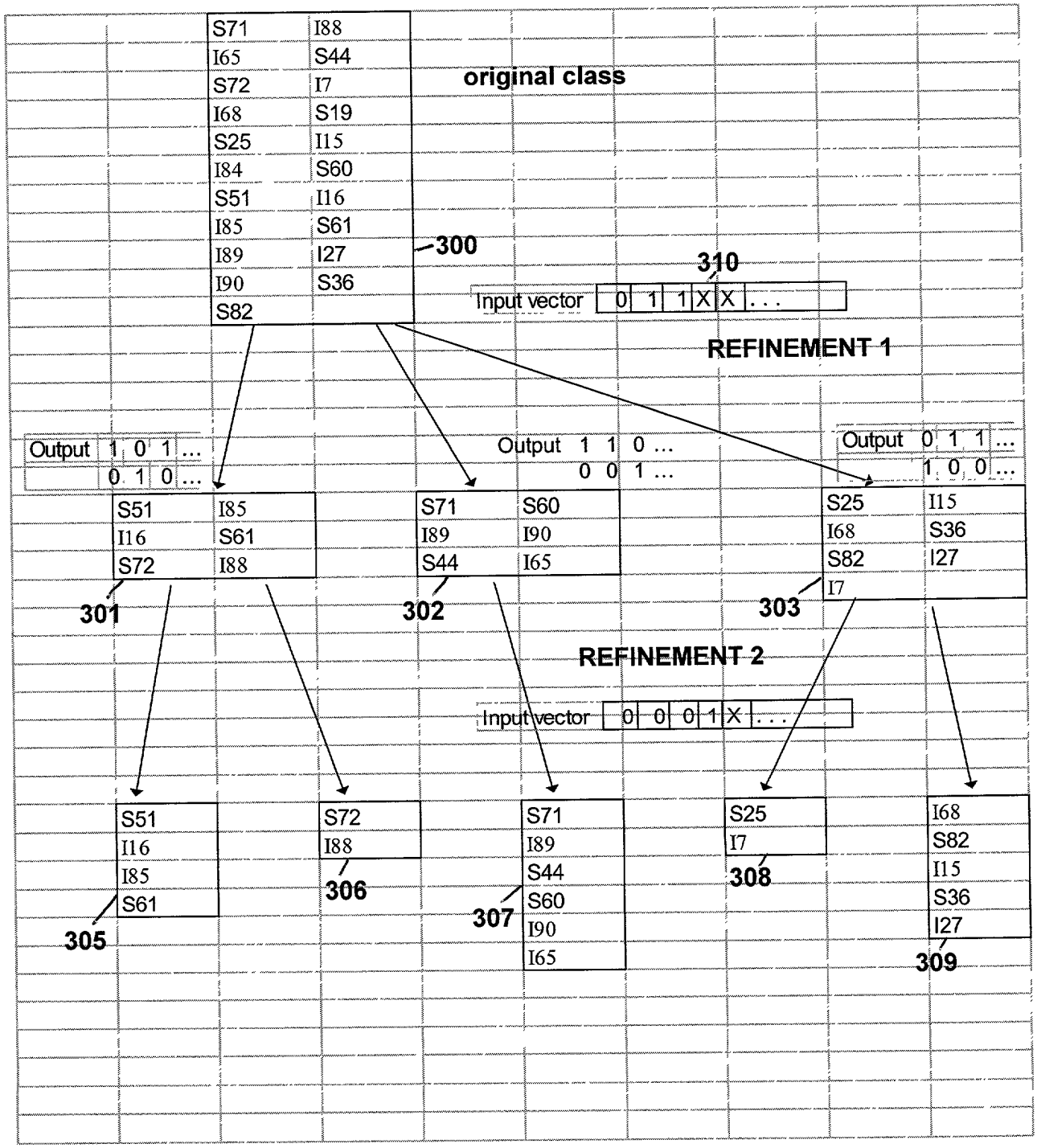
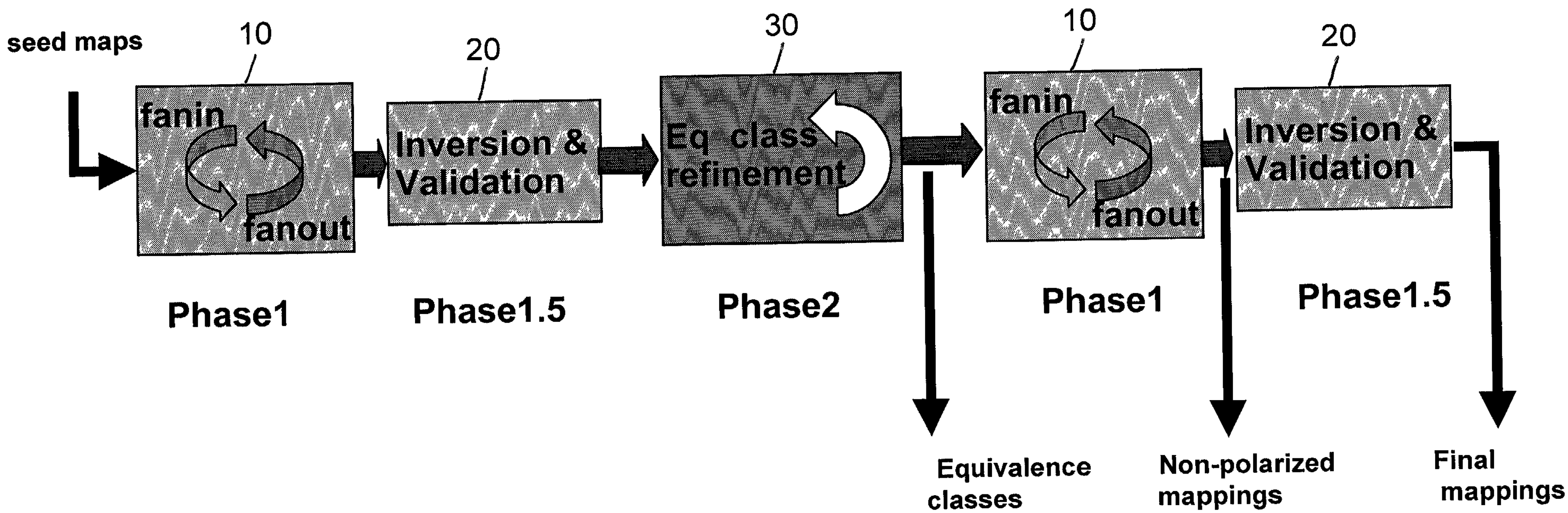

S71 I88
I65 S44
S72 I7
I68 S19
S25 I15
I84 S60
S51 I16
I85 S61
I89 I27
I90 S36
S82
original class
300
310
Input vector 0 1 1 X X . . .
REFINEMENT 1
Output 1 0 1 ...
0 1 0 ...
Output 1 1 0 ...
0 0 1 ...
Output 0 1 1 ...
1 0 0 ...
S51 I85
I16 S61
S72 I88
301
S71 S60
I89 I90
S44 I65
302
S25 I15
I68 S36
S82 I27
I7
303
REFINEMENT 2
Input vector 0 0 0 1 X . . .
S51
I16
I85
S61
305
S72
I88
306
S71
I89
S44
S60
I90
I65
307
S25
I7
308
I68
S82
I15
S36
I27
309

FIG. 8


seed maps
10
fanin
fanout
Phase1
20
Inversion &
Validation
Phase1.5
30
Eq class
refinement
Phase2
10
fanin
fanout
Phase1
20
Inversion &
Validation
Phase1.5
Equivalence
classes
Non-polarized
mappings
Final
mappings